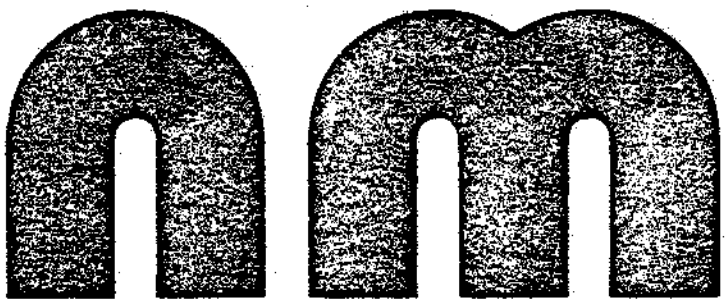

Nascom Microcomputers

# NASCOM

# MEMORY BOARD

# CONSTRUCTION NOTES

---

121 HIGH STREET
BERKHAMSTED HERTS

Tel: (04427) 74343
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CONTENTS PAGE



Supplied Seperately

Nascom Memory Board Functional Specification

# IMPORTANT

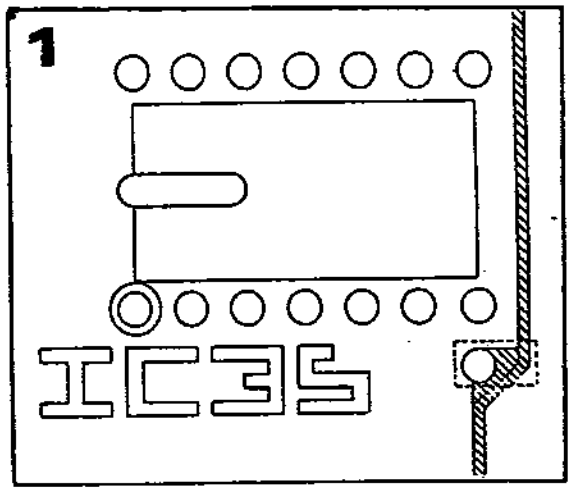
NASCOM RAM BOARD - PCB MODIFICATION

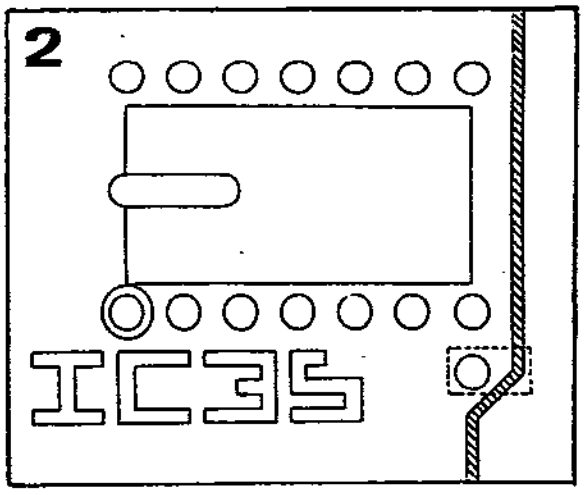
This RAM board has been etched in a manner that does not make a connection necessary for the operation of 4116 devices. Should it be required of the board that these devices be supported, a modification should be made as follows:

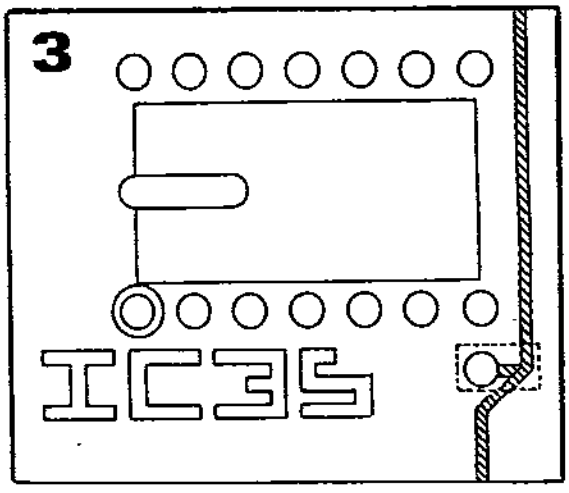
The through-plated hole affected is approximately 2mm from pin 7 of IC35 (see diagrams). It is shown enclosed by a dotted rectangle. The hole should have been connected to the track passing immediately to its right (board in normal orientation; diagram 1). The unmodified board is shown in diagram 2.

It is recommended that the solder resist covering the area enclosed by the dotted rectangle be removed by scraping with a small blade, and that, with a very small piece of wire OR a conductive film deposition agent such as RS silver paint, a link be made between track and hole as in diagram 3.

This modification need be implemented only in the case of boards supporting 4116 devices; 8K boards do not need the link to be added.

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Tools Needed

1. Long nose pliers
2. Side cutters
3. Soldering iron/bits. (The maximum bit size advisable for use on the integrated circuits is 1/16", although a 1/8" bit could be used on the component leads).
4. A damp sponge or cloth - to keep the soldering iron bit clean.
5. A powerful light source - for example, an angle-poise lamp.
6. A magnifying glass may prove useful.

Preliminary

1. Unpack kit and check components against the parts list. Brackets ( ) are provided along side the list to tick as the components are checked. Do not handle the memory devices (4027/4116) any more than is necessary. If possible check them in their antistatic packing; if not, return them to their packing immediately after checking.
2. Inspect the printed circuit board carefully for signs of damage.
3. Read carefully through all literature provided before beginning construction.
4. Note that no additional flux should be used with the resin-core solder provided.
5. The component side of the double-sided through-plated printed circuit board is identified by the silk-screening. The other side, with the gold-plated edge connector, is the side on which all soldering is to take place.
6. Brackets ( ) are provided alongside the various stages of the construction guide to assist in checking off each stage of assembly. Grid references are also given to assist in locating each device, and refer to the diagram on page 5 .

PARTS LIST - ALL MEMORY KITS

Integrated Circuits

| CHECK | NO.USED | TYPE | PINS | CIRCUIT REF. | DESCRIPTION |
|---|---|---|---|---|---|
| ( ) | 1 | 74LS00 | 14 | IC37 | Quad.2 input NAND gate |
| ( ) | 2 | 7402 | 14 | IC32,33 | Quad.2 input NOR gate |
| ( ) | 1 | 74LS04 | 14 | IC34 | Hex inverter |
| ( ) | 1 | 7406 | 14 | IC35 | Hex inverter buffer driver |
| ( ) | 1 | 74LS20 | 14 | IC36 | Dual 4 input NAND gate |
| ( ) | 1 | 74LS74 | 14 | IC31 | Dual D type flip-flop |
| ( ) | 1 | 74LS75 | 16 | IC25 | Quad bristable latch |
| ( ) | 2 | 74LS156 | 16 | IC22,23 | Dual 1 of 4 decoder |
| ( ) | 1 | 74LS139 | 16 | IC24 | Dual 1 of 4 decoder |
| ( ) | 2 | 74157 | 16 | IC20,21 | Quad 2 input multiplexer |
| ( ) | 1 | 74LS367 | 16 | IC3 | Hex buffer (tri-state) |
| ( ) | 3 | 81LS97 | 20 | IC1,2,26 | Octal buffer (tri-state |

Resistors

(All ¼ Watt, 5% Tolerance, High Stability Carbon Film)

| CHECK | NO.USED | VALUE | CIRCUIT REF. | MARKING |
|---|---|---|---|---|
| ( ) | 9 | 33R (33 ohms) | R7,8,9,10,11, 12,13,14,17 | OR/OR/BLK/GOLD |
| ( ) | 4 | 1KO(1.0k ohms) | R1,2,15,16 | BRN/BLK/RED/GOLD |
| ( ) | 1 | 2k2 | R5 | RED/RED/RED/GOLD |
| ( ) | 1 | 4k7 | R6 | YLW/PUR/RED/GOLD |

CAPACITORS

| CHECK | NO.USED | VALUE | CIRCUIT REF. | TYPE |
|---|---|---|---|---|
| ( ) | 11 | 10nF | - | Ceramic disc |
| ( ) | 40 | 100nF (=0.1uF) | A,B,C, | Ceramic disc |
| ( ) | 4 | 2.2uF | D,E | Tantalum Bead |

Sockets

| CHECK | NO.USED | TYPE | CIRCUIT REF. |
|---|---|---|---|
| ( ) | 7 | 14 Pin | IC.31-37 |
| ( ) | 23 | 16 Pin | IC. 3-25 |
| ( ) | 3 | 20 Pin | IC. 1,2,26 |
| ( ) | 4 | 24 Pin | IC.27-30 |

Miscellaneous

| CHECK | NO. | DESCRIPTION |
|---|---|---|
| ( / ) | 1 | 8" x 8" double sided through plated printed circuit board with solder resist mask on both sides and silk screening on component side. |
| ( / ) | 1 | 80 Way connector |
| ( / ) | 1 | length of 22 gauge solder with multicore flux. |

Parts list - Options

8k Memory kit - As basic, plus:

| CHECK | NO. | TYPE | PINS | CIRCUIT REF. | DESCRIPTION |
|---|---|---|---|---|---|
| ( ) | 16 | 4027 | 16 | IC's 4-11, 12-19 | 4096 bit dynamic RAM |

16k Memory kit - As basic, plus:

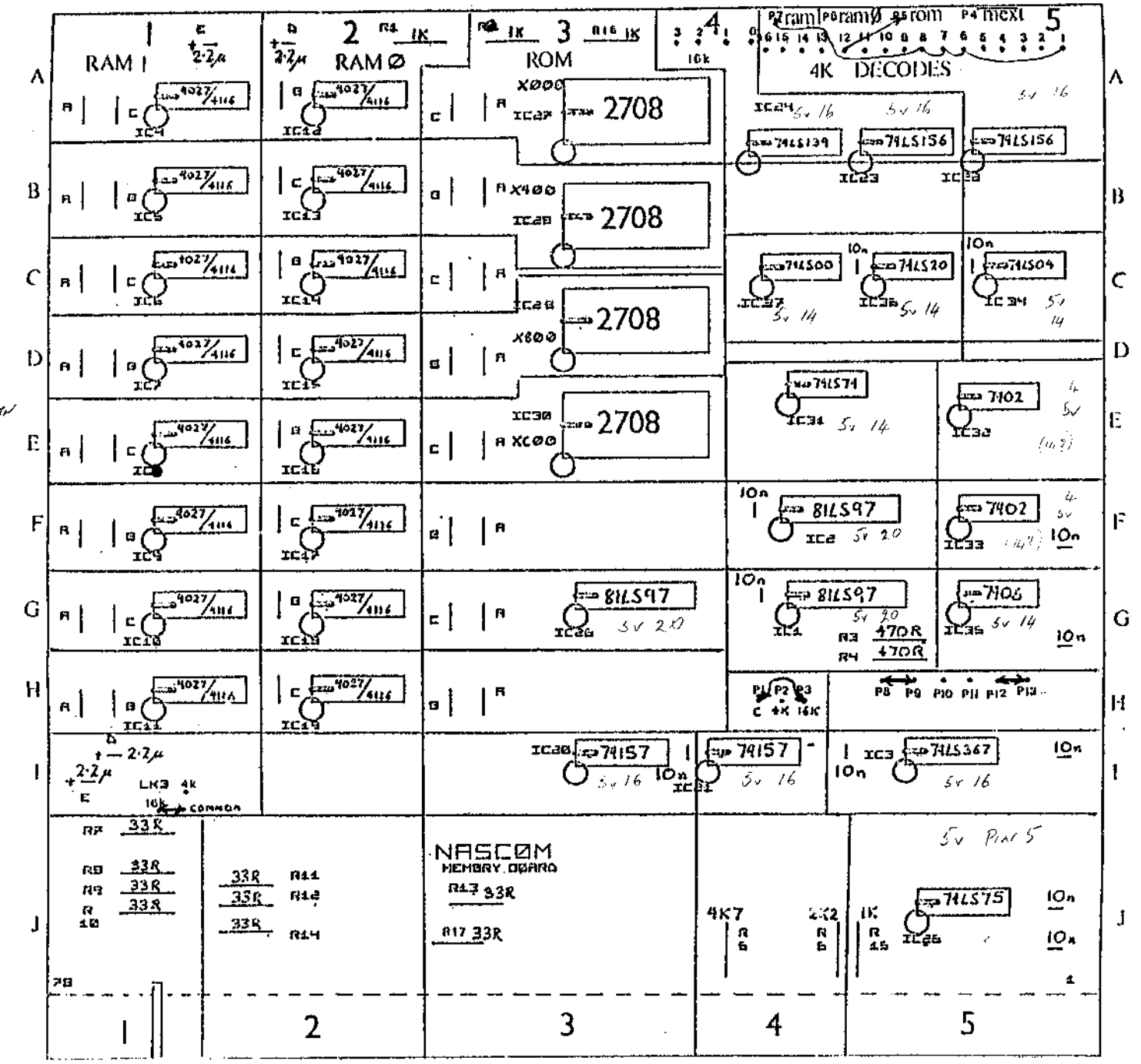
| | | | | | |
|---|---|---|---|---|---|
| ( ) | 8 | 4116 | 16 | IC's 4-11 | 16,384 bit dynamic RAM |

32k Memory kit - As 16k memory kit plus:

| | | | | | |
|---|---|---|---|---|---|
| ( ) | 8 | 4116 | 16 | IC's12-19 | 16,384 bit dynamic RAM |

EPROM options

| | | | | | |
|---|---|---|---|---|---|
| ( ) | Up to 4 | 2708 | 24 | IC's27-30 | 8x1024 bit EPROM |




CHECK FROM CONNECTION OF DC CAP

P6 - 2,3,4,13

## Construction

### Resistors

All resistors may be inserted either way round. They may be prepared for soldering by bending the leads to a separation of ½". This can be done with the aid of long nose pliers. care being taken not to damage the component by bending leads too close to the component body. After soldering, leads should be cut off about 0.1" from the underside of the board.

| Check | Resistor No. | Value | Colour Code | Board location |
|---|---|---|---|---|
| ( ) | R1 | 1KO | BRN/BLK/RED/GOLD | A2 |
| ( ) | R2 | 1KΩ | BRN/BLK/RED/GOLD | A3 |
| | *R3 | 470R | YLW/PUR/BRN/GOLD | G4 |
| | *R4 | 470R | YLW/PUR/BRN/GOLD | G4 |
| ( ) | R5 | 2K2 | RED/RED/RED/GOLD | J4 |
| ( ) | R6 | 4K7 | YLW/PUR/RED/GOLD | J4 |
| ( ) | R7 ) | | | |
| ( ) | R8 ) | 33R | OR/OR/BLK/GOLD | J1 |
| ( ) | R9 ) | | | |
| ( ) | R10) | | | |
| ( ) | R11) | 33R | OR/OR/BLK/GOLD | J2 |
| ( ) | R12) | | | |
| ( ) | R13 | 33R | OR/OR/BLK/GOLD | J3 |
| ( ) | R14 | 33R | OR/OR/BLK/GOLD | J2 |
| ( ) | R15 | 1Ko | BRN/BLK/RED/GOLD | J5 |
| ( ) | *R16* | 1KO | BRN/BLK/RED/GOLD | A3 |
| ( ) | R17 | 33R | OR/OR/BLK/GOLD | J3 |

*These resistors are not supplied, as they are not required for the 4027 or 4116 dynamic RAMs. They should be fitted only for memory devices requiring a +12V RAS signal.

*On the PCB there are three through plated holes in line with the silk-screen legend for R16. The two outside holes should be used for mounting R16.

### Links

There are several links on the board to select between the various types of memory device and to locate the memory blocks at various locations. See "Link Options" on page 10 for a fuller description of these.

| CHECK | | DESCRIPTION | BOARD LOCATION |
|---|---|---|---|
| ( ) | 68R | Link 1 - RAS option (normally P8-P9) | H5 |
| ( ) | 68R | Link 2 - RAS option (normally P12-P13) | H5 |
| ( ) | | Link 3 - 4K/16K device select | I1 |
| ( ) | | Link 4 - 4K/16K device select | H4 |
| ( ) | | P4 Nascom 1 MEXT select | A5 |
| ( ) | | P5 4K ROM block select | A5 |
| ( ) | | P6 RAMs IC12-19 select | A5 |
| ( ) | x | P7 RAMS IC4-11 select | A5 |

## I.C. Sockets

On the PCB pin 1 of each I.C. is indicated by a circle at one corner. All integrated circuits are mounted with the same orientation. Pin 1 of each socket is usually indicated by orientation marks in the plastic moulding. When inserting the sockets take care not to bend any pins.

| Check | Socket No. | No. of pins | Board location |
|---|---|---|---|
| ( ) | 1,2 | 20 | G5, F5 |
| ( ) | 3 | 16 | I5 |
| ( ) | 4-11 | 16 | A1-H1 |
| ( ) | 12-19 | 16 | A2-H2 |
| ( ) | 20,21 | 16 | I3, I4 |
| ( ) | 22-24 | 16 | A5, A4, A4 |
| ( ) | 25 | 16 | J5 |
| ( ) | 26 | 20 | G3 |
| ( ) | 27-30 | 24 | A3-E3 |
| ( ) | 31-35 | 14 | E4, E5, F5, C5, G5 |
| ( ) | 36, 37 | 14 | C4 |

## Capacitors

All capacitors (apart from the four tantalum bead electrolytics) may be inserted either way round. The four tantalum capacitors are mounted with the plus sign or other marking facing away from the edge of the board with the gold-plated edge connector. If a multi-meter is available all capacitors should be tested for short circuits before insertion.

| Check | Value | Board marking | Board location |
|---|---|---|---|
| ( ) | 2.2u F Tantalum | D | A2 |
| ( ) | | E | A1 |
| ( ) | | D, E | I1 |
| ( ) | 10n F Ceramic | - | C4, C5, F4, F5 |
| ( ) | | | G4, G5, I3 |
| ( ) | | | I5, I5, J5, J5 |
| ( ) | 100n F Ceramic | A, B, C | 2 x A1-H1 |
| ( ) | | | 2 x A3-H3 |
| ( ) | | B, C | A2-H2 |

Note: The markings (ABCDE) on the board denote which supply rail the capacitor is decoupling.

A=0.1u 0V to + 5V
B=0.1u 0V to + 12V
C=0.1u 0V to - 5V
D=2.2u 0V to -5V
E=2.2u 0V to + 12V

The mark (-) denotes a 10uF capacitor. 0V to + 5V

( ) Test 1 At this stage the memory board should be plugged into the Nasbus and the power switched on (see "power requirements" on page 11 ). The voltages of the nasbus should be checked to ensure that there are no short circuits on the board between the supply rails. The power should then be switched off and the board removed from the nasbus.

TTL Integrated Circuits.

All integrated circuits are mounted with the same orientation. On the PCB, pin 1 of each I.C. is indicated by a circle in one corner. Each IC has pin 1 indicated either by a small nick in the corresponding end of the IC or a circular mark close to pin one.

| Check | Circuit Ref. | I.C.Type | Board Location |
|---|---|---|---|
| ( ) | IC1 | 81LS97 | G4 |
| ( ) | IC2 | 81LS97 | F4 |
| ( ) | IC3 | 74LS367 | I5 |
| ( ) | IC20 | 74157 | I3 |
| ( ) | IC21 | 74157 | I4 |
| ( ) | IC22 | 74LS156 | A5 |
| ( ) | IC23 | 74LS156 | A4 |
| ( ) | IC24 | 74LS139 | A4 |
| ( ) | IC25 | 74LS75 | J5 |
| ( ) | IC26 | 81LS97 | G3 |
| ( ) | IC31 | 74LS74 | E4 |
| ( ) | IC32 | 7402 | E5 |
| ( ) | IC33 | 7402 | F5 |
| ( ) | IC34 | 74LS04 | C5 |
| ( ) | IC35 | 7406 | G5 |
| ( ) | IC36 | 74LS20 | C4 |
| ( ) | IC37 | 74LS00 | C4 |

( ) Test 2. The decoding can be partially tested at this stage. First of all link 5 on the NASCOM 1 should be changed from internal memory to external memory. The memory card should be plugged into the NASBUS and the system powered up. The screen should clear, with the prompt and cursor in the bottom left hand corner as normal. All commands should operate as normal. However, instead of the NASCOM 1 4K memory block being repeated every 4K, it should appear only once, from 0000 to 0FFF. Therefore, tabulating 0 to 60 will give the first 96 bytes of NASBUG (i.e. 31 33 ØC 21 etc) whereas tabulating 1000 to 1060, 2000 to 2060, etc.. will not any more.

( ) Switch off the power and remove the memory board.

Memory devices

The dynamic RAMs supplied with the memory kit are MOS devices and the MOS IC handling precautions outlined in the NASCOM 1 Construction Notes (Page 28, Note 4) should be adhered to. These are expensive devices and great care should be taken with them.

8K or 32K Option

( ) The 16 memory I.C's (4027 or 4116) should be inserted in IC positions 4-11 and 12-19.

16K Option

( ) The 8 memory I.C's (4116) should be inserted in IC positions 4-11.

The memory board is now complete and can be plugged into the NASBUS for final testing. Comprehensive test routines are listed in the Appendix.

## APPENDIX 1

### Link Options

A full description of all link functions and address selection is given in the Memory Card Functional Specification. Listed below is a summary of the linking required for each memory board option, and the recommended addressing structure for the first memory card in an expanded system.

### 8K Memory Board (16 x 4027)

| | | |
|---|---|---|
| Link 1 - RAS option | P8-P9 | |
| Link 2 - RAS option | P12-P13 | |
| Link 3 - 4K/16K device select | Common - 4K | |
| Link 4 - 4K/16K " " | P1-P2 | |
| Nascom MEM select | P4-5 | (0000 - 0FFF) |
| 4K Rom Block select | P5-~~12~~ 10 | (F000 - FFFF) |
| RAMs IC4-11 select | P7-6 | (1000 - 1FFF) |
| RAMs IC12-19 select | P6-7 | (2000 - 2FFF) |

### 16K Memory Board (8 x 4116)

| | | |
|---|---|---|
| Link 1 - RAS option | P8-P9 | |
| Link 2 - RAS option | P12-P13 | |
| Link 3 - 4K/16K device select | Common - 16K | |
| Link 4 - 4K/16K " " | P1-P3 | |
| Nascom MEM select | P4-5 *for nascom 2* | (0000 - 0FFF) |
| 4K Rom Block select | P5-~~12~~ 10 | (~~F000~~ - ~~FFFF~~) (D000 - DFFF) |
| RAMs IC4-11 select | P7-6,7,8,1 | (1000 - 4FFF) |

### 32K Memory Board (16 x 4116)

As 16K above plus:

| | | |
|---|---|---|
| RAMs IC12-19 select | P6-2,3,4,13 | (5000 - 8FFF) |

# APPENDIX II

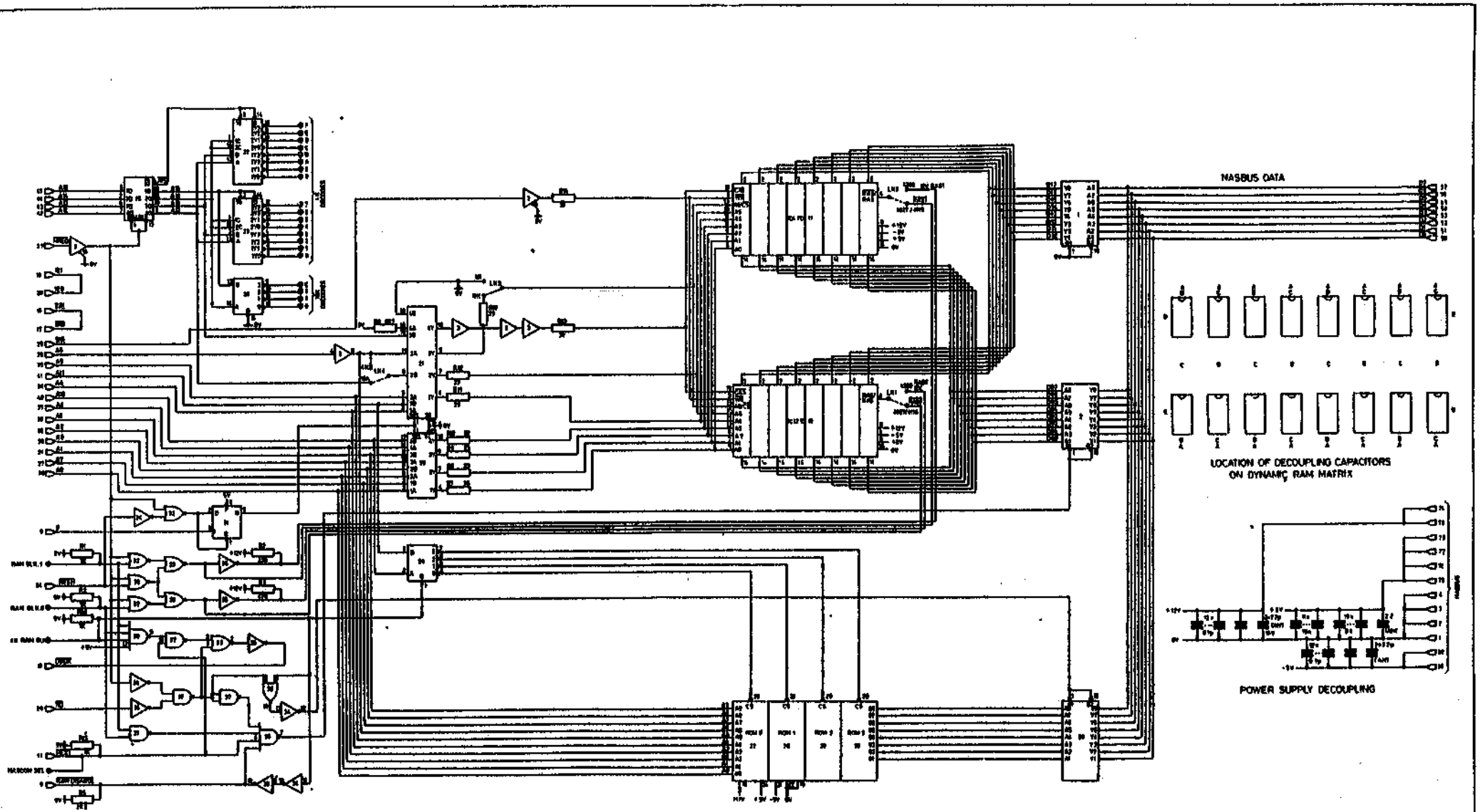
## Power Requirements

The power requirements for a Nascom 1 with extended memory are listed below:

| | | |
|---|---|---|
| Nascom 1 | +12V | 100mA |
| ( with 2 EPROMS) | + 5V | 820mA |
| | - 5V | 40mA |
| | -12V | 15mA |
| Buffer Board | + 5V | 200mA |

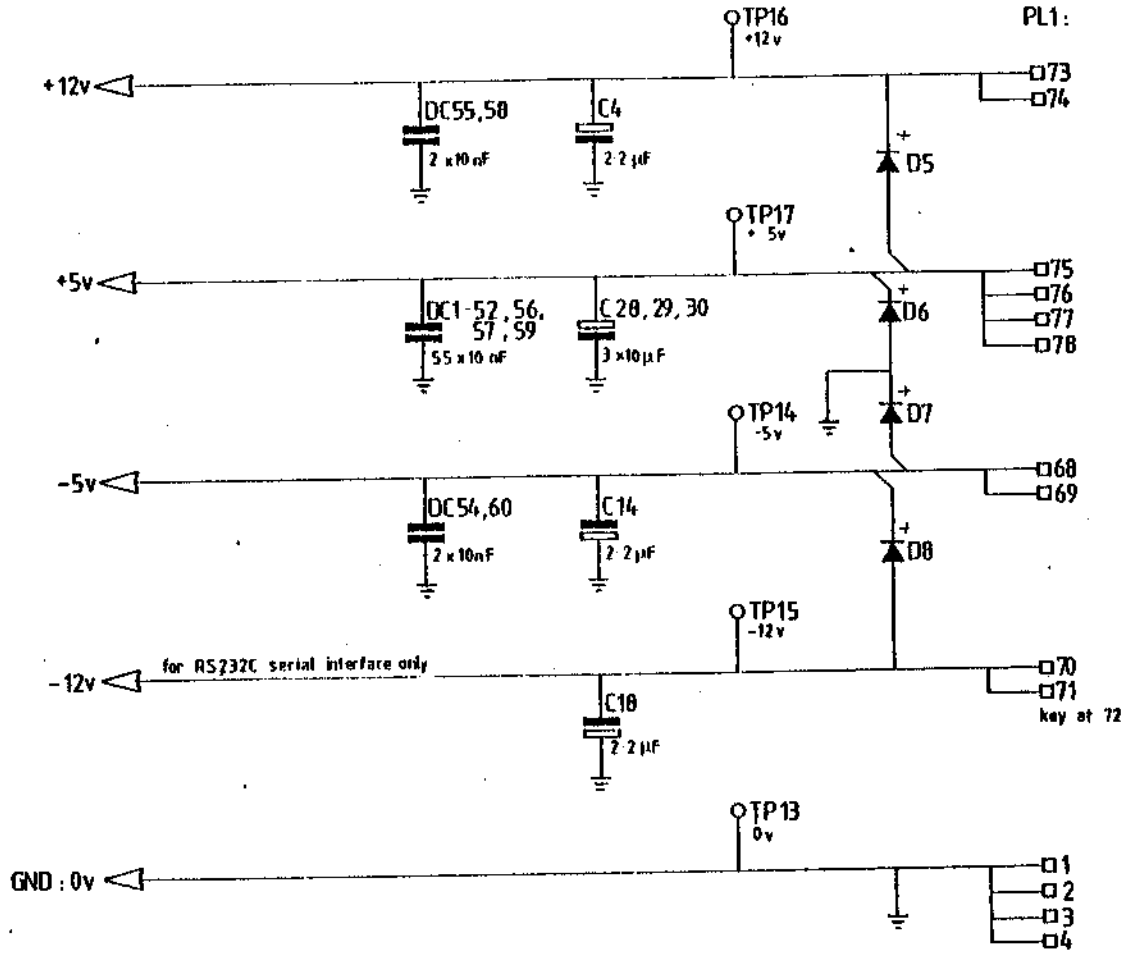
Ram Board

| | | |
|---|---|---|
| with 32K and 4K EPROMS | +12V | 200mA |
| | + 5V | 170mA |
| | - 5V | 70mA |




NASCOM MICROCOMPUTERS

RAM/BOARD




D5-7: 4 x 1N4001

| | | | | | | |
|---|---|---|---|---|---|---|
| Nascom Microcomputers<br>121 High Street Berkhamsted Herts | NASCOM 2-Power Distribution | Issue 6 | Sht 5 of 5 | Drawn | Checked | Date 11·10·79 |
| | | Revisions: | | | Drawing no. 4·022·103 | |

## 4. SUMMARY OF WIRE LINK OPTIONS

### 4.1 4k/16 select

| | | | |
|---|---|---|---|
| For 4k chips | Link P1 to P2 | Link 3 | Common to 4k |
| For 16k chips | Link P1 to P3 | Link 3 | Common to 16k |

### 4.2 Memory Block Selects

| | | |
|---|---|---|
| P4 | Nascom MEM | select NOT REQUIRED FOR NASCOM 2 |
| P5 | 4k ROM block | select |
| P6 | RAMS IC 12-19 | select |
| P7 | RAMS IC 4-11 | select |

### 4.3 Row Address Strobe options

| | | | | |
|---|---|---|---|---|
| For 'normal' | RAS | (4027/4116) | ICs 4-11 | Link P12-13 68K |
| For 'normal' | RAS | (4027/4116) | ICs 12-19 | Link P 9-P8 68K |
| For + 12V | RAS | | ICs 4-11 | Link P12-P11 |
| For +12V | RAS | | ICs 12-19 | Link P 9-P10 |

TABLE 3.1

4k memory decode pads

| Pad No. | 4k Block Memory Address (Hexadecimal) |
|---|---|
| 1 | 4000-4FFF |
| 2 | 5000-5FFF |
| 3 | 6000-6FFF |
| 4 | 7000-7FFF |
| 5 | 0000-0FFF |
| 6 | 1000-1FFF |
| 7 | 2000-2FFF |
| 8 | 3000-3FFF |
| 9 | C000-CFFF |
| 10 | D000-DFFF |
| 11 | E000-EFFF |
| 12 | F000-FFFF |
| 13 | 8000-8FFF |
| 14 | 9000-9FFF |
| 15 | A000-AFFF |
| 16 | B000-BFFF |

TABLE 3.2

16k memory decode pads

| Pad No. | 16k Block Memory Address (Hexadecimal) |
|---|---|
| 0 | 0000-3FFF |
| 1 | 4000-7FFF |
| 2 | 8000-BFFF |
| 3 | C000-FFFF |

TABLE 3.3

'Wired-OR' Address Selection for 16k Chips

| Memory Block Addresses (Hexadecimal) | 4k decodes linked together |
|---|---|
| 0000-3FFF | 5,6,7,8 |
| 1000-4FFF | 6,7,8,1 |
| 2000-5FFF | 7,8,1,2 |
| 3000-6FFF | 8,1,2,3 |
| 4000-7FFF | 1,2,3,4 |
| 5000-8FFF | 2,3,4,13 |
| 6000-9FFF | 3,4,13,14 |
| 7000-AFFF | 4,13,14,15 |
| 8000-BFFF | 13,14,15,16 |
| 9000-CFFF | 14,15,16,9 |
| A000-DFFF | 15,16,9,10 |
| B000-EFFF | 16,9,10,11 |
| C000-FFF | 9,10,11,12 |

## APPENDIX III

### Memory Tests NOT NASCOM 2 (CALLS TO MONITOR NEED ALTERING)

Attached are two test routines to verify correct operation of the memory.

The first test writes into each location of memory a byte which is related to the address of that location and then checks, byte by byte, that the same data reads back. This test therefore checks that each byte is uniquely addressable.

The second test writes all 256 byte combinations (i.e. OO to FF) into each memory location and checks that the same data reads back. This test therefore checks that every bit of the memory can be set or reset.

### Execution

After loading either program , execution is started by typing:

ED00 XXXX YYYY ( New line)

where XXXX is the address of the first location to be tested, and YYYY the address of the last location.;

Note that these tests destroy any data or program in the tested memory area.

After either program has cycled through the specified memory once, an asterisk "*" will be printed on the screen to indicate that one 'pass' has been completed. The test is repeated indefinitely until the user resets the Nascom.

### Error Printouts

If an error is found the following printout occurs:

AAAA EE DD

where AAAA is the address of the byte in error, EE is the data written to that address (and expected back), and DD is the actual data read back. A delay of approximately one second is included in the error printout.

### Program running indicator

When testing a large amount of memory both programs will run a long time before printing the first asterisk. The program should therefore be tested on a small area of memory (say OEOO to OE2O), before testing the complete memory board.

During running the first memory test routine has a "program running indicator" which appears in the centre of the screen on the top line. This takes the form of a O alternating with a ⊙ and so gives the impression of a O with a dot flashing in the centre of it.

```
                        0001 ;
                        0002 ;          MEMORY TEST PROGRAM FOR NASCOM
                        0003 ;          BASED ON TEST IN MOSTEK 1978
                        0004 ;          MEMORY DATA BOOK & DESIGNERS
                        0005 ;          GUIDE PAGE 225.
                        0006 ;
0000'                   0007            ORG 0D00H
0D00  0600              0008 TEST:      LD      B,0     ;PATTERN MODIFIER
0D02  3E4F              0009            LD      A,4FH   ;SET UP SCREEN FLAG
0D04  32E00B            0010            LD      (0BE0H),A  ;PUT IT THERE
0D07  2A0E0C            0011 LOOP:      LD      HL,(0C0EH)  ;GET START ADDRESS
0D0A  ED5B100C          0012            LD      DE,(0C10H)  ;GET END ADDRESS
0D0E  13                0013            INC     DE      ;DE=END+1
0D0F  7D                0014 PUTIN:     LD      A,L     ;CALCULATE DATA
0D10  AC                0015            XOR     H       ; FROM ADDRESS &
0D11  A8                0016            XOR     B       ; PATTERN MODIFIER
0D12  77                0017            LD      (HL),A  ;PUT IT IN MEMORY
0D13  23                0018            INC     HL      ;INC POINTER
0D14  B7                0019            OR      A       ;CLEAR CARRY
0D15  ED52              0020            SBC     HL,DE   ;COMPARE HL & DE
0D17  19                0021            ADD     HL,DE
0D18  20F5              0022            JR      NZ,PUTIN  ;Z MEANS WE'VE DONE
0D1A  2A0E0C            0023            LD      HL,(0C0EH)  ;GET START AGAIN
0D1D  7D                0024 RDBACK:    LD      A,L     ;CALCULATE DATA
0D1E  AC                0025            XOR     H       ; FROM ADDRESS &
0D1F  A8                0026            XOR     B       ; PATTERN MODIFIER
0D20  4F                0027            LD      C,A     ;SAVE IN C
0D21  7E                0028            LD      A,(HL)  ;GET DATA FROM MEMORY
0D22  B9                0029            CP      C       ;SEE IF IT'S OK
0D23  C43C0D            0030            CALL    NZ,ERROR  ;ANY ERRORS?
0D26  23                0031            INC     HL      ;INC POINTER
0D27  B7                0032            OR      A       ;CLEAR CARRY
0D28  ED52              0033            SBC     HL,DE   ;COMPARE HL & DE
0D2A  19                0034            ADD     HL,DE
0D2B  20F0              0035            JR      NZ,RDBACK  ;Z MEANS WE'VE DONE
0D2D  3AE00B            0036            LD      A,(0BE0H)  ;GET SCREEN FLAG
0D30  EE40              0037            XOR     40H     ;TO SHOW ACTIVITY
0D32  32E00B            0038            LD      (0BE0H),A  ;PUT IT BACK
0D35  10D0              0039            DJNZ    LOOP    ;CHANGE PATTERN MODIFIER
0D37  EF                0040            RST     28H     ;PRINT A '*' FOR
0D38  2A00              0041            DB      '*',0   ;END OF PASS
0D3A  18C4              0042            JR      TEST    ;DO IT ALL AGAIN
                        0043 ;
                        0044 ;          ERROR PRINTOUT
                        0045 ;
                        0046 ;          ADDR  EXPECTED FOUND
                        0047 ;
0D3C  E5                0048 ERROR:     PUSH    HL      ;SAVE ALL REGISTERS
0D3D  D5                0049            PUSH    DE
0D3E  C5                0050            PUSH    BC
0D3F  F5                0051            PUSH    AF
0D40  7C                0052            LD      A,H     ;A=HI BYTE OF ADDR
0D41  CD4402 1903       0053            CALL    244H    ;PRINT IT IN HEX
0D44  7D                0054            LD      A,L     ;A=LO BYTE OF ADDR
0D45  CD4402 1903       0055            CALL    244H    ;PRINT IT IN HEX
0D48  CD3C02 0603       0056            CALL    23CH    ;SPACE
0D4B  79                0057            LD      A,C     ;A=EXPECTED DATA
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0D4C  CD4402 1903       0058            CALL    244H    ;PRINT IT IN HEX
0D4F  CD3C02 0603       0059            CALL    23CH    ;SPACE
0D52  F1                0060            POP     AF      ;A=DATA FOUND
0D53  CD4402 1903       0061            CALL    244H    ;PRINT IT IN HEX
0D56  CD4002 1103       0062            CALL    240H    ;NEW LINE
0D59  010000            0063            LD      BC,0    ;DELAY LOOP
0D5C  0B                0064 WAIT:      DEC     BC      ;COUNT DOWN BC
0D5D  78                0065            LD      A,B     ; UNTIL ZERO
0D5E  B1                0066            OR      C
0D5F  20FB              0067            JR      NZ,WAIT
0D61  C1                0068            POP     BC      ;RESTORE REGS
0D62  D1                0069            POP     DE
0D63  E1                0070            POP     HL
0D64  C9                0071            RET
0D65  (0000)            0072            END
```

```
                        0001 ;
                        0002 ;       MEMORY TEST PROGRAM FOR NASCOM
                        0003 ;
0000'                   0004         ORG 0D00H
0D00  0E00              0005 MTEST:  LD      C,0              ;C HOLDS DATA
0D02  2A0E0C            0006 OUTER:  LD      HL,(0C0EH)       ;GET START ADDRESS
0D05  ED5B100C          0007         LD      DE,(0C10H)       ;GET END ADDRESS
0D09  13                0008         INC     DE
0D0A  79                0009 INNER:  LD      A,C
0D0B  77                0010         LD      (HL),A           ;PUT INTO MEMORY
0D0C  46                0011         LD      B,(HL)
0D0D  B8                0012         CP      B
0D0E  C4220D            0013         CALL    NZ,ERROR
0D11  23                0014         INC     HL
0D12  B7                0015         OR      A
0D13  ED52              0016         SBC     HL,DE
0D15  19                0017         ADD     HL,DE
0D16  20F2              0018         JR      NZ,INNER         ;KEEP FILLING
0D18  0C                0019         INC     C
0D19  79                0020         LD      A,C
0D1A  B7                0021         OR      A                ;SET FLAGS
0D1B  20E5              0022         JR      NZ,OUTER
0D1D  EF                0023         RST     28H
0D1E  2A00              0024         DB      '*',0
0D20  18E0              0025         JR      OUTER
                        0026 ;
                        0027 ;       ERROR PRINTOUT
                        0028 ;
                        0029 ;       ADDR  EXPECTED FOUND
                        0030 ;
0D22  E5                0031 ERROR:  PUSH    HL
0D23  D5                0032         PUSH    DE
0D24  C5                0033         PUSH    BC
0D25  7C                0034         LD      A,H
0D26  CD4402 1903       0035         CALL    244H
0D29  7D                0036         LD      A,L
0D2A  CD4402 1903       0037         CALL    244H
0D2D  CD3C02 0603       0038         CALL    23CH
0D30  79                0039         LD      A,C              ;EXPECTED
0D31  CD4402 1903       0040         CALL    244H
0D34  CD3C02 0603       0041         CALL    23CH
0D37  78                0042         LD      A,B              ;FOUND
0D38  CD4402 1903       0043         CALL    244H
0D3B  CD4002 1103       0044         CALL    240H
0D3E  010000            0045         LD      BC,0
0D41  0B                0046 WAIT:   DEC     BC
0D42  78                0047         LD      A,B
0D43  B1                0048         OR      C
0D44  20FB              0049         JR      NZ,WAIT
0D46  C1                0050         POP     BC
0D47  D1                0051         POP     DE
0D48  E1                0052         POP     HL
0D47  C9                0053         RET
0D4A  (0000)            0054         END

Errors                  0
```

MEMORY PLAGUE

"Memory Plague" is a euphamism for the unexplained failure of about 10% of Nascom memory boards, and its causes are to say the least obscure. It would seem that noise caused by switching transients from the data latches (81LS97) and the address multiplexers (74LS157) may be breaking onto the data bus via IC2. Board layout may be to blame, in conjunction with chips that just happen to be on the low side of average for noise immunity.

Identifying "Memory Plague" is not as easy as it would at first appear because a memory suffering from mild plague may pass both memory test programs in the construction manuals with flying colours and run Tiny Basic with little difficulty. This is because both memory tests and Tiny Basic are loading operands to memory, and not actually executing M1 (op-code fetch) cycles. M1 cycles are more critical on timing and hence more suseptible to corruption caused by noise. Likewise "Memory modify" and "Copy" commands are unlikely to cause problems except in severe cases. So the only thing likely to reveal "Memory Plague" is a program with lots of M1 cycles and filling a sizeable chunk of memory. ZEAP is ideal for this. If you do not have ZEAP, then write a simple relocatable program that may be copied throughout memory, finishing with the printing of an * then looping back to the start. Leave this running as long as possible. If the program "crashes", then provided you have eliminated mains noise as the cause, then its likely that "Plague" has struck.

None of the cures for this are technically elegant, but they do work. They should be tried in order until the problem is cured. Don't go in for overkill, as this is unnecessary and undesirable.

1. Go for a National 81LS97 in the IC2 position (AMD devices seem to have lower noise immunity although AMD deny this). You have 7 81LS97s in total, 3 on the Nascom, 1 on the buffer, and 3 on the memory. One of these at least is likely to be made by National. Swap these ICs about for the best results in the IC2 position.

2. Grid off the Ground and +5 volt supplies. On the underside of the pcb it will be noted that the GND and +5V rails supplying the TTL ICs terminate at the end of each row. Wire links can be fitted to connect these rails to the equivalent rails supplying the RAM chips, thus completing the "grid" on the power supply rails, thereby reducing power supply noise. Take care not to short out the power supply rails by "gridding" to the wrong tracks.

3. The 74LS04 on the buffer board may be replaced with a 74S04. Unfortunately this increases the loading on the Z80 but it does tidy up the MREQ waveform.

4. On ICs4-11 only, fit a 4K7 resistors from pin 9 to pin 14 of each chip, thus pulling the outputs of the RAMs to +5V.

5. On ICs4-11 only, in addition to 4 (above), fit 47pF ceramic capacitors from pin 14 to pin 16, thus producing a time constant on the RAM output.

Various combinations of these cures have been tried with 100% success on the faulty boards that we have examined and, although not 'elegant' solutions, they have transformed unreliable memory boards into fully functional units.

All Nascom Distributors are aware of these problems and if you have any difficulty they will be more than willing to assist you in finding a solution.